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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,286	06/27/2003	Abbas Ali	TI-31505A	8530

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EXAMINER	
VINH, LAN	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 11/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,286	ALI ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☒ Claim(s) *18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/17/2005 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-6, 13-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "said dielectric layer" in line 8. There is insufficient antecedent basis for this limitation in the claim since it is unclear which dielectric layer, the first or the second dielectric layer that "said dielectric layer" refers to

Claims 2-6 are indefinite because they depend on claim 1

Claim 13 recites the limitation "the dielectric layer" in line 7. There is insufficient antecedent basis for this limitation in the claim since it is unclear which dielectric layer, the first or the second dielectric layer that "the dielectric layer" refers to

Claims 14-18 are indefinite because they depend on claim 13

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-3, 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chao et al (US 6,429,119) in view of Yu et al (US 6,458,689)

Chao discloses a process for manufacturing dual damascene. This process comprises the steps of:

providing a silicon substrate 10 containing conductive line 12 (col 7 lines 34-36; fig. 2), which reads on providing a silicon substrate containing one or more electronic devices

forming a first dielectric layer 17 over the substrate 10, layer 17 having a thickness/first thickness (col 7, lines 60-63; fig. 2)

forming a first etch stop layer 18 (SiN) over dielectric layer 17/first dielectric layer (col 8, lines 1-5; fig. 3)

forming a second dielectric layer 19 over the first dielectric layer 17, layer 19 having a thickness (col 8, lines 10-12, fig. 2)

etching a first trench in the dielectric layer 19/second dielectric layer (col 8, lines 35-40; fig.3)

etching at the same time a second trench having a depth in the second dielectric layer 19 and the first trench in the first dielectric layer 17 (col 8, lines 45-50 and fig. 4, fig. 4 shows that the depth of second trench/second depth is approximately equal to the thickness of second dielectric layer 19

forming a barrier/liner film in the first and second trench (col 8, lines 55-60)

forming a contacting/conductive copper layer filling both first and second trenches (col 8, lines 56-65)

Unlike the instant claimed inventions as per claims 1-2, Chao fails to disclose the step of forming an ARC layer of SiON over the second dielectric ate prior to etching the trench

Yu discloses a method for forming a semiconductor structure comprises the step of forming an ARC layer of SiON over the dielectric layer prior to etching the trench (col 4, lines 19-22; fig. 3-4)

Since Chao is concerned with a step of CMP the trench structure (col 8, lines 60-62), one skilled in the art at the time the invention was made would have found it obvious to modify Chao method by adding the step of forming an ARC layer of SiON over the dielectric layer prior to etching the trench as per Yu because Yu discloses that the ARC layer fills the microcratches and the ARC is an excellent stop layer that prevent a subsequent CMP process from scratching the underlying dielectric layer (col 4, lines 31-38)

The limitations of claims 3, 6 have been discussed above

4. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chao et al (US 6,429,119) in view of Yu et al (US 6,458,689) and further in view Gabriel et al (US 6,475,929)

Chao as modified by Yu has been described above. Chao and Yu differs from the instant claimed inventions as per claims 4-5 by forming the first and second dielectric layers of silicon oxide instead of FSG (Fluorosilicate glass)

However, Gabriel in a method of forming dual damascene,discloses that a dielectric layer can be formed of silicon oxide or FSG (col 7, lines 25-28)

Hence, one skilled in the art would have found it obvious to substitute Chao silicon oxide dielectric layer with FSG in view of Gabriel teaching because Gabriel discloses that the silicon oxide and FSG are material capable of acting as a dielectric layer (col 7, lines 25-27)

5. Claims 7-9, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chao et al (US 6,429,119) in view of Yu et al (US 6,458,689)

Chao discloses a process for manufacturing dual damascene. This process comprises the steps of:

providing a silicon substrate 10 containing conductive line 12 (col 7 lines 34-36; fig. 2), which reads on providing a silicon substrate containing one or more electronic devices

forming a first dielectric layer 17 over the substrate 10, layer 17 having a thickness/first thickness (col 7, lines 60-63; fig. 2)

forming a first etch stop layer 18 (SiN) over dielectric layer 17/first dielectric layer (col 8, lines 1-5; fig. 3)

forming a second dielectric layer 19 over the first dielectric layer 17, layer 19 having a thickness (col 8, lines 10-12, fig. 2)

etching a first trench in the dielectric layer 19/second dielectric layer and the first dielectric layer 17, the first trench having a depth that is greater than the thickness of the layer 19/second dielectric (col 8, lines 35-40; fig.3)

etching at the same time a second trench having a depth in the second dielectric layer 19 and the first trench in the first dielectric layer 17 (col 8, lines 45-50 and fig. 4, fig. 4 shows that the depth of second trench/second depth is approximately equal to the thickness of second dielectric layer 19

forming a barrier/liner film in the first and second trench (col 8, lines 55-60)

forming a contacting/conductive copper layer filling both first and second trenches (col 8, lines 56-65)

Unlike the instant claimed inventions as per claim 7, Chao fails to disclose the step of forming an ARC layer of SiON over the second dielectric ate prior to etching the trench

Yu discloses a method for forming a semiconductor structure comprises the step of forming an ARC layer of SiON over the dielectric layer prior to etching the trench (col 4, lines 19-22; fig. 3-4)

Since Chao is concerned with a step of CMP the trench structure (col 8, lines 60-62), one skilled in the art at the time the invention was made would have found it obvious to modify Chao method by adding the step of forming an ARC layer of SiON over the dielectric layer prior to etching the trench as per Yu because Yu discloses that the ARC layer fills the microcratches and the ARC is an excellent stop layer that prevent a subsequent CMP process from scratching the underlying dielectric layer (col 4, lines 31-38)

Regarding claim 8, one skilled in the art at the time the invention was made would have found it obvious that Chao and Yu silicon oxynitride ARC layer would have had the atomic percent numbers as recited in claim 8 because the atomic percent numbers are physical propedies of SiON (see prior art of record for evidence of this basis)

The limitations of claims 9, 12 have been discussed above

6. Claims 10-11, 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chao et al (US 6,429,119) in view of Yu et al (US 6,458,689) and further in view Gabriel et al (US 6,475,929)

Chao as modified by Yu has been described above. Chao and Yu differs from the instant claimed inventions as per claims 10-11, 16-17 by forming the first and second dielectric layers of silicon oxide instead of FSG (Fluorosilicate glass)

However, Gabriel in a method of forming dual damascene,discloses that a dielectric layer can be formed of silicon oxide or FSG (col 7, lines 25-28)

Hence, one skilled in the art would have found it obvious to substitute Chao silicon oxide dielectric layer with FSG in view of Gabriel teaching because Gabriel discloses that the silicon oxide and FSG are material capable of acting as a dielectric layer (col 7, lines 25-27)

7. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chao et al (US 6,429,119) in view of Yu et al (US 6,458,689)

Chao discloses a process for manufacturing dual damascene. This process comprises the steps of:

providing a silicon substrate 10 containing conductive line 12 (col 7 lines 34-36; fig. 2), which reads on providing a silicon substrate containing one or more electronic devices

forming a first etch stop 16 over the substrate (fig. 3)

forming a first dielectric layer 17 over the etch stop 16 (col 7, lines 60-63; fig. 2)

forming a second etch stop layer 18 (SiN) over dielectric layer 17/first dielectric layer (col 8, lines 1-5; fig. 3)

forming a second dielectric layer 19 over the second etch stop 18 (col 8, lines 10-12, fig. 2)

etching a first trench through the dielectric layer 19/second dielectric layer and the second etch stop 18 (col 8, lines 35-40; fig.3)

etching at the same time a second trench having a second width greater than the width of the first trench in the second dielectric layer down to the second etch stop 18 and etching the first trench through the first dielectric layer 17 down to the first etch stop 16/46, wherein the second trench overlies the first trench (col 8, lines 45-52; fig. 4)

Unlike the instant claimed inventions as per claims 13-14, Chao fails to disclose the step of forming an ARC layer of SiON over the second dielectric layer prior to etching the first trench

Yu discloses a method for forming a semiconductor structure comprises the step of forming an ARC layer of SiON over the dielectric layer prior to etching the trench (col 4, lines 19-22; fig. 3-4)

Since Chao is concerned with a step of CMP the trench structure (col 8, lines 60-62), one skilled in the art at the time the invention was made would have found it obvious to modify Chao method by adding the step of forming an ARC layer of SiON over the dielectric layer prior to etching the trench as per Yu because Yu discloses that the ARC layer fills the microcratches and the ARC is an excellent stop layer that prevent a

subsequent CMP process from scratching the underlying dielectric layer (col 4, lines 31-38)

The limitation of claim 15 has been discussed above

Allowable Subject Matter

8. Claim 18 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sim et al (US 6,423,654) discloses that SiON has an atomic composition ratio of silicon (25-40%), oxygen (25-40%), nitrogen (25-40%) (abstract)

Response to Arguments

10. Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LV
November 5, 2005